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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,005	06/14/2001	Michio Horiuchi	149-01	5592
7590		05/17/2004		
Paul & Paul 2900 Two Thousand Market Street Philadelphia, PA 19103			EXAMINER OWENS, DOUGLAS W	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/881,005

Applicant(s)

HORIUCHI ET AL.

Examiner

Douglas W Owens

Art Unit

2811

*an*

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 4-18 is/are pending in the application.
- 4a) Of the above claim(s) 6-10,17 and 18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,11,13 and 16 is/are rejected.
- 7) ☒ Claim(s) 5,12,14 and 15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date: \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Objections*

1. Claim 11 is objected to because of the following informalities: in line 5, the phrase "the circuit board" should be replaced with the phrase "one of the circuit boards of said plurality of circuit boards", or a similar phrase because there is no antecedent basis for the term, "the circuit board". Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4 and 11, 13 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,128,831 to Fox, III et al.

Regarding claims 1 and 16, Fox, III et al. teaches a multi-layered semiconductor device characterized in that a film-like semiconductor package (Figs. 1 – 3) incorporating therein a semiconductor chip (15) disposed in a package accommodation opening of a circuit pattern layer to form a circuit board, said circuit pattern layer comprises a substrate (11), a circuit pattern formed on the substrate, and said package accommodation opening, and a plurality of such circuit boards are layered together to

electrically connect said circuit patterns of the respective circuit boards with each other, wherein the electrical connection between the circuit patterns on the respective circuit boards is performed via a low melting point metal filled in a through hole formed in the semiconductor package (Col. 5, lines 35 – 47) to establish an interlayer connection.

Regarding claims 2 and 13, Fox, III et al. teaches a semiconductor device, wherein every adjacent board is bonded to another with an insulation adhesive (Col. 5, lines 16 – 24) except for an electrically connected portion. Although, Fox, III et al. does not explicitly state that the adhesive is insulative, it is an inherent feature, since a conductive adhesive would introduce the danger of undesired shorting between traces.

Regarding claim 4, Fox, III et al. teaches a semiconductor device, wherein the electrical connection between the circuit patterns is performed by connecting an extension of the circuit pattern into a hole (17) formed in the package (See Fig. 1, for example).

Regarding claim 11, Fox, III et al. teaches a semiconductor device formed of a plurality of circuit boards layered together (Fig. 3), each circuit board comprising an insulation substrate (11), a semiconductor chip (15) in the substrate, a circuit formed on the surface of the substrate and connected to the chip characterized in that a lead extending from one of the circuit boards is bonded to a circuit on another circuit board disposed beneath the former circuit board to establish an interlayer connection (Col. 5, lines 42 – 45), said lead extending through a through-hole in the insulation substrate of the former circuit board (Col. 3, lines 16 – 25).

***Allowable Subject Matter***

4. Claims 5, 12, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

5. Applicant's arguments with respect to claims 1, 2, 4, 5, and 11 – 16 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. This application contains claims 6 – 10, 17 and 18 drawn to an invention nonelected with traverse in Paper No. 5. A complete reply to the final rejection must

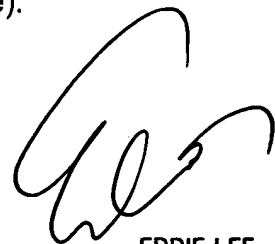
include cancellation of nonelected claims or other appropriate action (37 CFR 1.144)  
See MPEP § 821.01.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DWO



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800